1.8 Ω Maximum On Resistance, ±15 V/12 V/±5 V, *i*CMOS, Dual SPDT Switch

Preliminary Technical Data

ADG1436

FEATURES

- 1.8 Ω maximum on resistance at 25°C
- 0.37 Ω maximum on-resistance flatness
- 0.17 Ω maximum on-resistance match between channels
- Continuous current per channel
  - LFCSP package: 300 mA
  - TSSOP package: 240 mA
- Fully specified at +12 V, ±15 V, and ±5 V
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 16-lead TSSOP and 4 mm × 4 mm, 16-lead LFCSP packages

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Communication systems
- Relay replacement

FUNCTIONAL BLOCK DIAGRAM

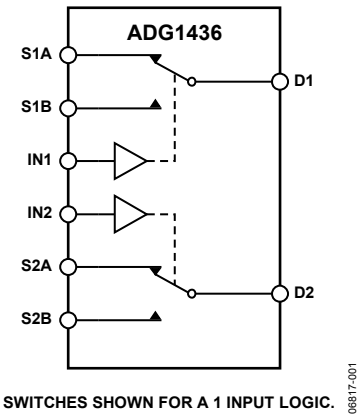

Figure 1. TSSOP Package

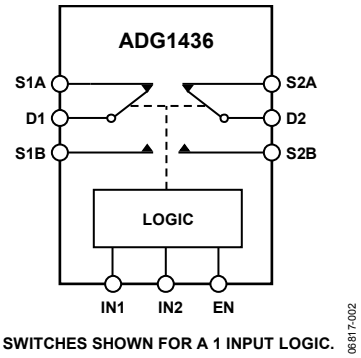

Figure 2. LFCSP Package

GENERAL DESCRIPTION

The ADG1436 is a monolithic CMOS device containing two independently selectable SPDT switches. An EN input on the LFCSP package is used to enable or disable the device. When disabled, all channels are switched off. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. Both switches exhibit break-before-make switching action for use in multiplexer applications.

The ADG1436 is designed on an *i*CMOS process. *i*CMOS (industrial-CMOS) is a modular manufacturing process combining high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals. *i*CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 2.5 Ω maximum on resistance over temperature.
2. Minimum distortion.
3. Ultralow power dissipation: <0.03 µW.
4. 16-lead TSSOP and 16-lead 4 mm × 4 mm LFCSP packages.

Rev. PrD
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SPECIFICATIONS

15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	1.5			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 24
	1.8	2.2	2.5	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels (ΔR_{ON})	0.1			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.13	0.16	0.17	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.28			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.31	0.35	0.37	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = ±10 V, V_S = ±10 V; see Figure 25
	±0.5	±10	±100	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = ±10 V, V_S = ±10 V; see Figure 25
	±0.5	±10	±100	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04			nA typ	V_S = V_D = ±10 V; see Figure 26
	±1	±10	±100	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	125			ns typ	R_L = 300 Ω, C_L = 35 pF
	170	215	245	ns max	V_S = +10 V; see Figure 31
t_{ON} (EN)	95			ns typ	R_L = 300 Ω, C_L = 35 pF
	120	140	155	ns max	V_S = 10 V; see Figure 31
t_{OFF} (EN)	105			ns typ	R_L = 300 Ω, C_L = 35 pF
	130	150	170	ns max	V_S = 10 V; see Figure 31
Break-Before-Make Time Delay, t_{BBM}	20			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = +10 V; see Figure 32
Charge Injection	-20			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 34
Off Isolation	-80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 27
Channel-to-Channel Crosstalk	-80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 28
Total Harmonic Distortion + Noise	0.011			% typ	R_L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz see Figure 30
−3 dB Bandwidth	110			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 29
Insertion Loss	-0.17			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
C_S (Off)	23			pF typ	f = 1 MHz, V_S = 0 V
C_D (Off)	50			pF typ	f = 1 MHz, V_S = 0 V
C_D, C_S (On)	120			pF typ	f = 1 MHz, V_S = 0 V
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.001			μA typ	Digital Inputs = 0 V or V_{DD}
			1	μA max	
I_{DD}	170			μA typ	Digital Input = 5 V
			230	μA max	
I_{SS}	0.001			μA typ	Digital Inputs = 0 V, 5 V, or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	GND = 0 V

[1] Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	3			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 24
	3.5	4.3	4.7	Ω max	V_{DD} = +10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels (ΔR_{ON})	0.12			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.16	0.18	0.2	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.85			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	1	1.13	1.16	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 25
	±0.5	±10	±100	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 25
	±0.5	±10	±100	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04			nA typ	V_S = V_D = 1 V or 10 V; see Figure 26
	±1	±10	±100	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	200			ns typ	R_L = 300 Ω, C_L = 35 pF
	270	320	350	ns max	V_S = 8 V; see Figure 31
t_{ON} (EN)	175			ns typ	R_L = 300 Ω, C_L = 35 pF
	235	280	310	ns max	V_S = 8 V; see Figure 31
t_{OFF} (EN)	105			ns typ	R_L = 300 Ω, C_L = 35 pF
	145	175	195	ns max	V_S = 8 V; see Figure 31
Break-Before-Make Time Delay, t_{BBM}	70			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 8 V; see Figure 32
Charge Injection	30			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 34
Off Isolation	-80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 27;
Channel-to-Channel Crosstalk	-80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 28
−3 dB Bandwidth	110			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 29
Insertion Loss	0.18			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
C_S (Off)	40			pF typ	f = 1 MHz, V_S = 6 V
C_D (Off)	80			pF typ	f = 1 MHz, V_S = 6 V
C_D, C_S (On)	140			pF typ	f = 1 MHz, V_S = 6 V
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{DD}	170			μA typ	Digital inputs = 5 V
			230	μA max	
V_{DD}			5/16.5	V min/max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design, not subject to production test.

5 V DUAL SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	3.5			Ω typ	V_S = ±4.5 V, I_S = −10 mA; see Figure 24
	4	4.8	5.3	Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On-Resistance Match Between Channels (ΔR_{ON})	0.12			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.16	0.18	0.2	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.88			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	1.1	1.2	1.3	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 25
	±0.5	±10	±100	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 25
	±0.5	±10	±100	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04			nA typ	V_S = V_D = ±4.5V; see Figure 26
	±1	±10	±100	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	310			ns typ	R_L = 300 Ω, C_L = 35 pF
	445	510	565	ns max	V_S = 3 V; see Figure 31
t_{ON} (EN)	255			ns typ	R_L = 300 Ω, C_L = 35 pF
	355	415	460	ns max	V_S = 3 V; see Figure 31
t_{OFF} (EN)	215			ns typ	R_L = 300 Ω, C_L = 35 pF
	305	355	400	ns max	V_S = 3 V; see Figure 31
Break-Before-Make Time Delay, t_{BBM}	80			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 3 V; see Figure 32
Charge Injection	30			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 34
Off Isolation	-80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 27
Channel-to-Channel Crosstalk	-80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 28
Total Harmonic Distortion + Noise	0.03			% typ	R_L = 110 Ω, 2.5 V pp, f = 20 Hz to 20 kHz see Figure 30
−3 dB Bandwidth	85			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 29
Insertion Loss	0.28			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
C_S (Off)	33			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	65			pF typ	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	145			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	GND = 0 V

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Ratings
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	600 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current per Channel, S or D	
16-Lead TSSOP	240 mA
16-Lead LFCSP	300 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance (4-layer board)	112°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance	30.4°C/W
Reflow Soldering Peak Temperature, Pb free	260(+0/−5)°C

[1] Over voltages at IN, S, and D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

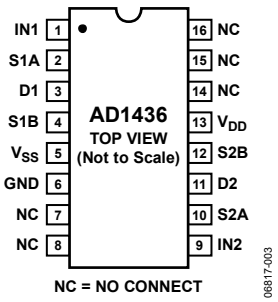

Figure 3.TSSOP Pin Configuration

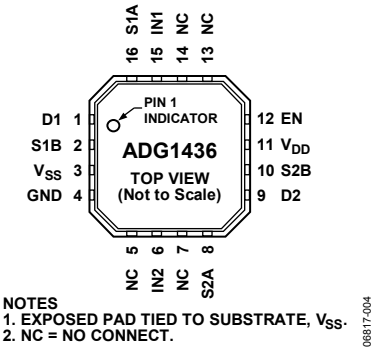

Figure 4. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Function**
1	15	IN1	Logic Control Input.
2	16	S1A	Source Terminal. Can be an input or output.
3	1	D1	Drain Terminal. Can be an input or output.
4	2	S1B	Source Terminal. Can be an input or output.
5	3	V_{SS}	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7, 8, 14 to 16	5, 7, 13, 14	NC	No Connect.
9	6	IN2	Logic Control Input.
10	8	S2A	Source Terminal. Can be an input or output.
11	9	D2	Drain Terminal. Can be an input or output.
12	10	S2B	Source Terminal. Can be an input or output.
13	11	V_{DD}	Most Positive Power Supply Potential.
N/A	12	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, INx logic inputs determine the on switches.

TRUTH TABLE FOR SWITCHES

Table 6. ADG1436 TSSOP Truth Table

INx	SxA	SxB
0	Off	On
1	On	Off

Table 7. ADG1436 LFCSP Truth Table

EN	INx	SxA	SxB
0	X	Off	Off
1	0	Off	On
1	1	On	Off

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminal D and Terminal S.

R_{ON}
The ohmic resistance between Terminal D and Terminal S.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, which is measured with reference to ground.

C_D (Off)
The off switch drain capacitance, which is measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, which is measured with reference to ground.

C_{IN}
The digital input capacitance.

$t_{TRANSITION}$

The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

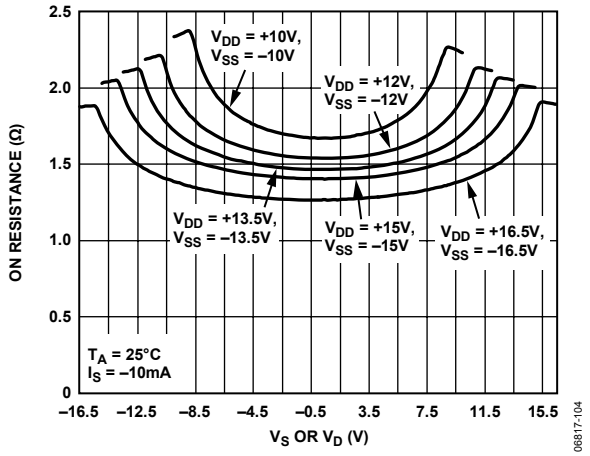

Figure 5. On Resistance as a Function of V_D (V_S), Dual Supply

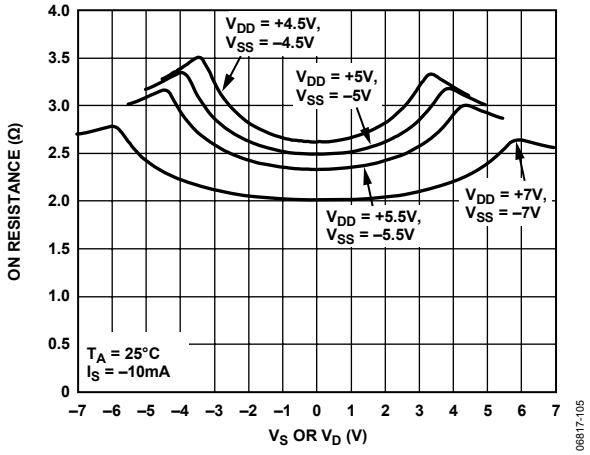

Figure 6. On Resistance as a Function of V_D (V_S), Dual Supply

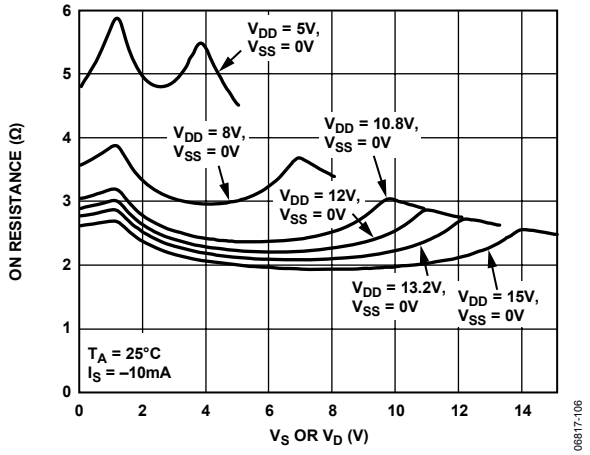

Figure 7. On Resistance as a Function of V_D (V_S), Single Supply

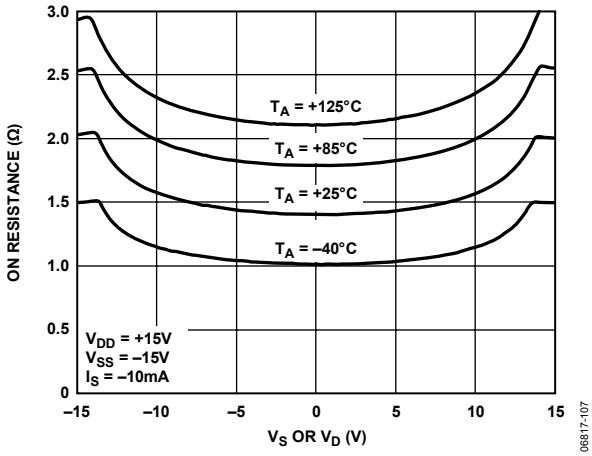

Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, 15 V Dual Supply

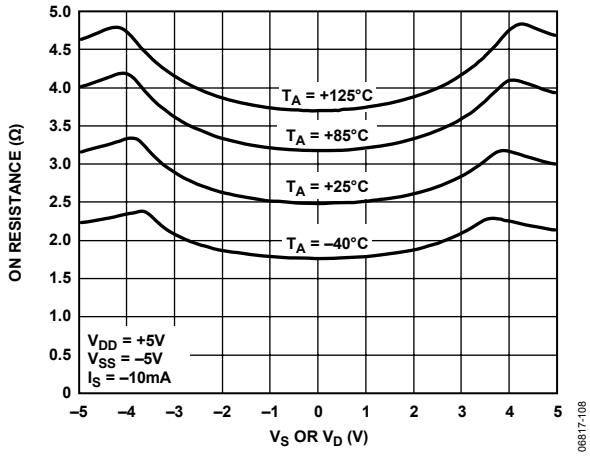

Figure 9. On Resistance as a Function of V_D (V_S) for Different Temperatures, 5 V Dual Supply

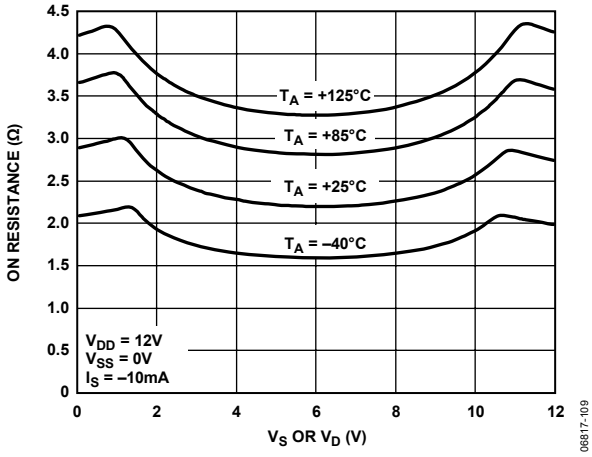

Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

Figure 11. Leakage Currents as a Function of Temperature, 15 V Dual Supply

Figure 12. Leakage Currents as a Function of Temperature, 15 V Dual Supply

Figure 13. Leakage Currents as a Function of Temperature, 5 V Dual Supply

Figure 14. Leakage Currents as a Function of Temperature, 12 V Single Supply

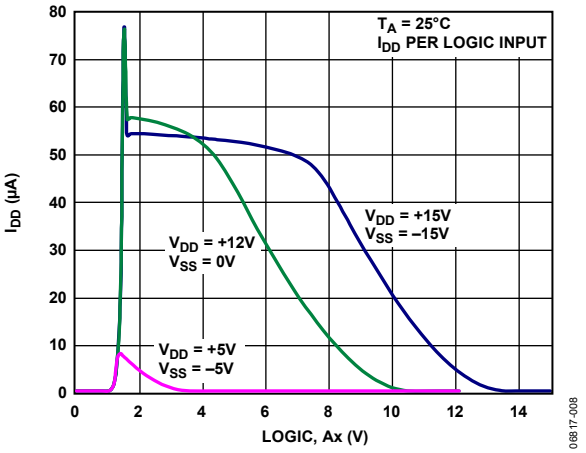

Figure 15. I_{DD} vs. Logic Level

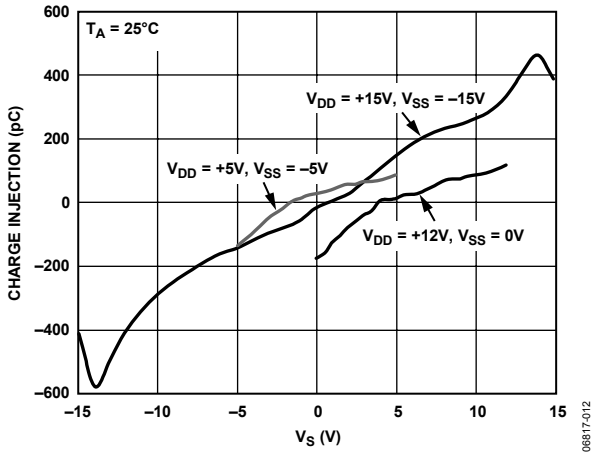

Figure 16. Charge Injection vs. Source Voltage

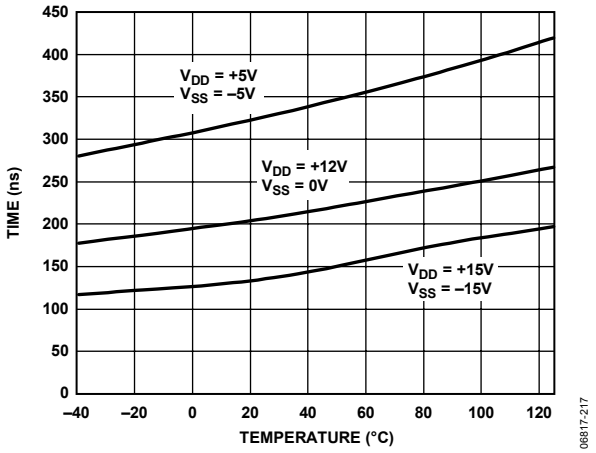

Figure 17. $t_{TRANSITION}$ Times vs. Temperature

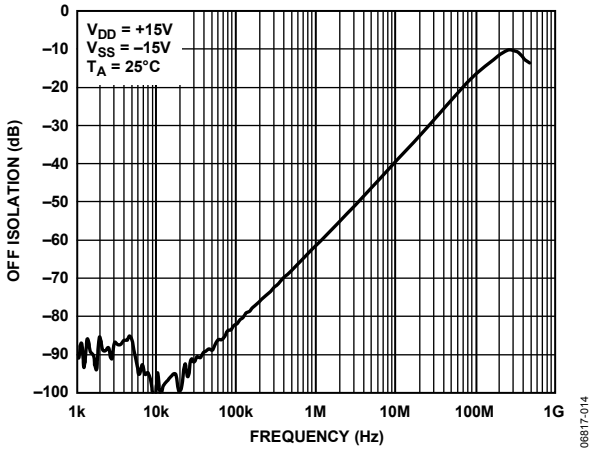

Figure 18. Off Isolation vs. Frequency

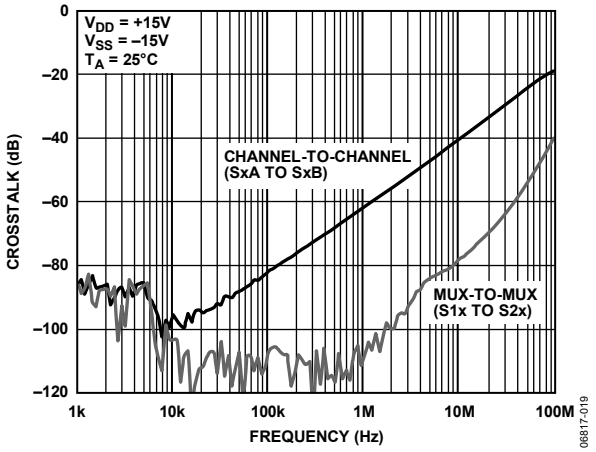

Figure 19. Crosstalk vs. Frequency

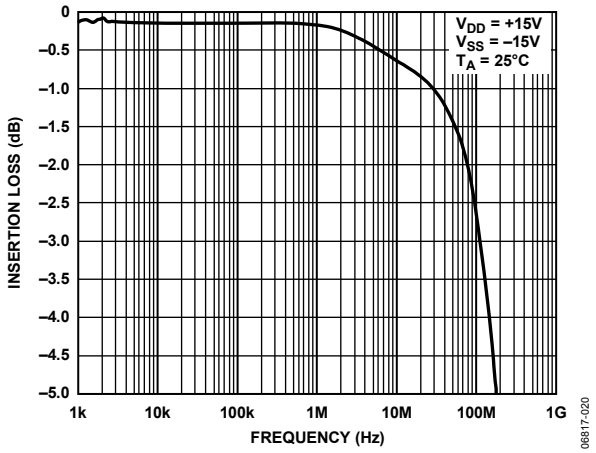

Figure 20. On Response vs. Frequency

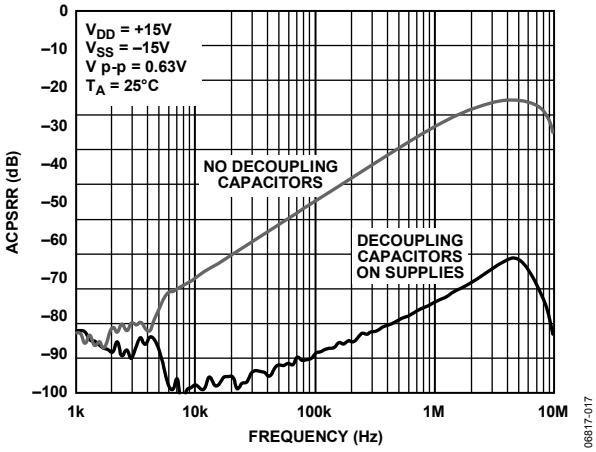

Figure 21. ACPSRR vs. Frequency

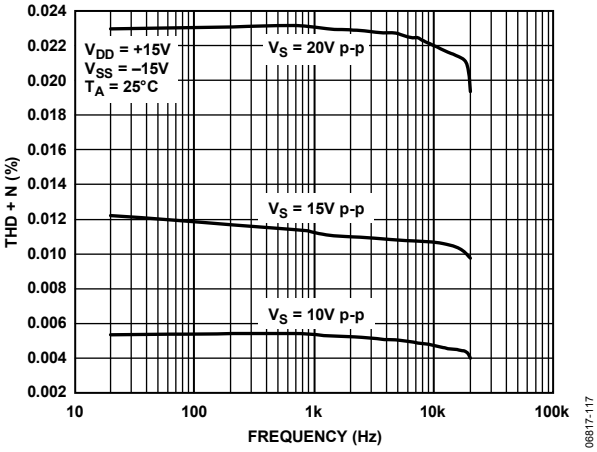

Figure 22. THD + N vs. Frequency, 15 V Dual Supply

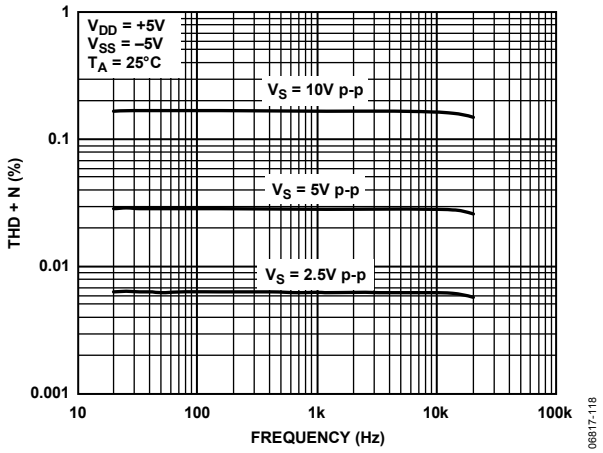

Figure 23. THD + N vs. Frequency, 5 V Dual Supply

TEST CIRCUITS

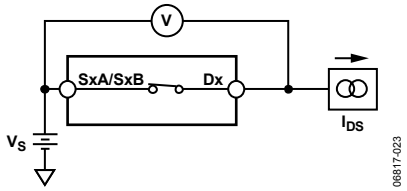

Figure 24. On Resistance

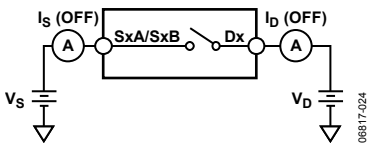

Figure 25. Off Leakage

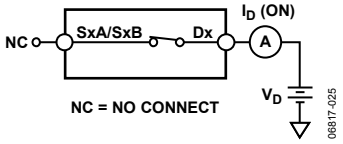

Figure 26. On Leakage

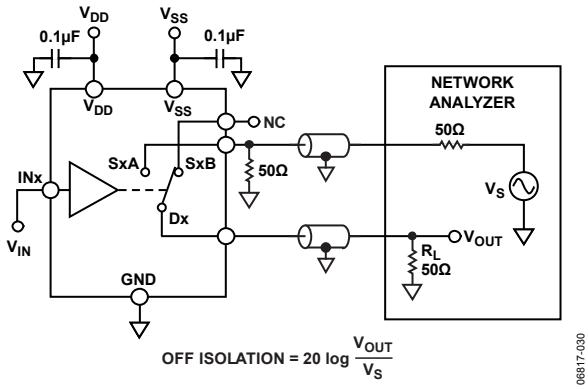

Figure 27. Off Isolation

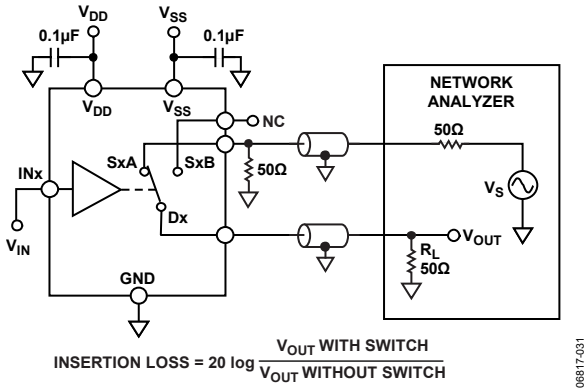

Figure 28. Channel-to-Channel Crosstalk

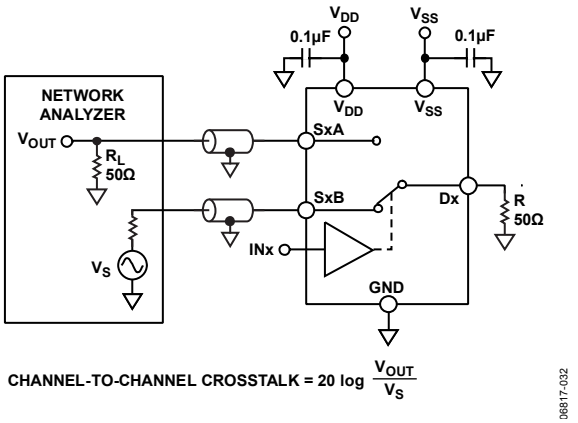

Figure 29. Bandwidth

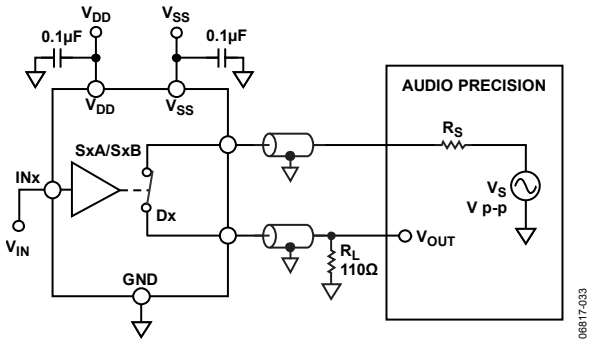

Figure 30. THD + Noise

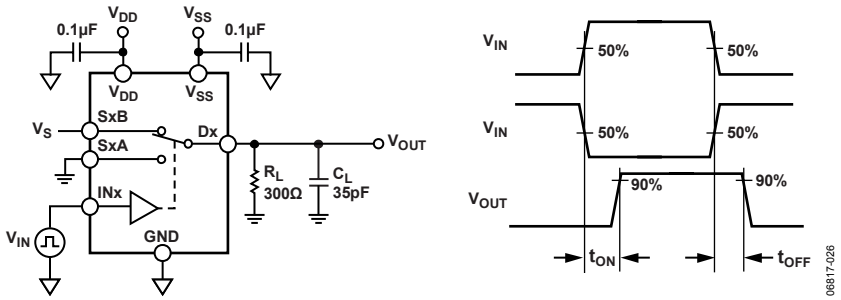

Figure 31. Switching Times

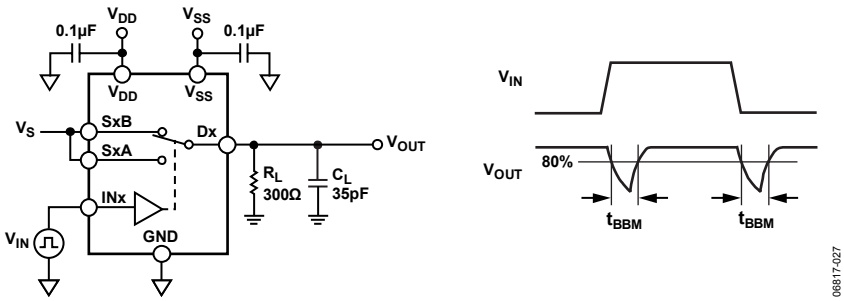

Figure 32. Break-Before-Make Time Delay

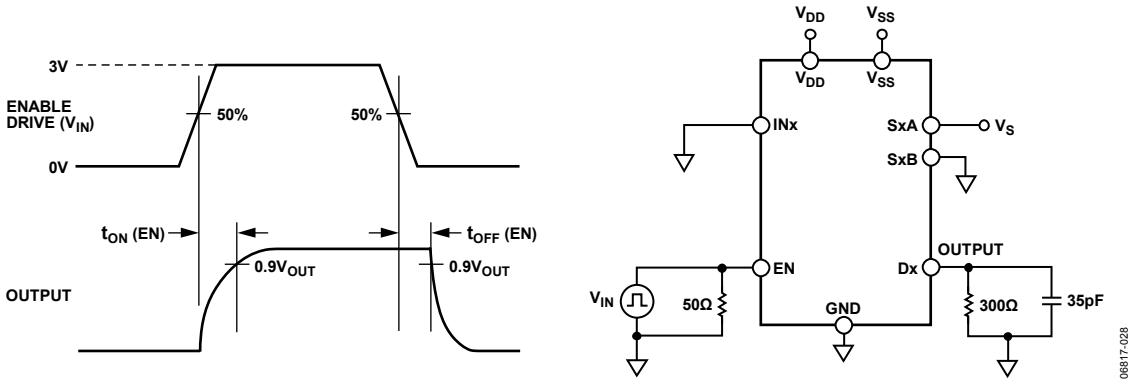

Figure 33. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

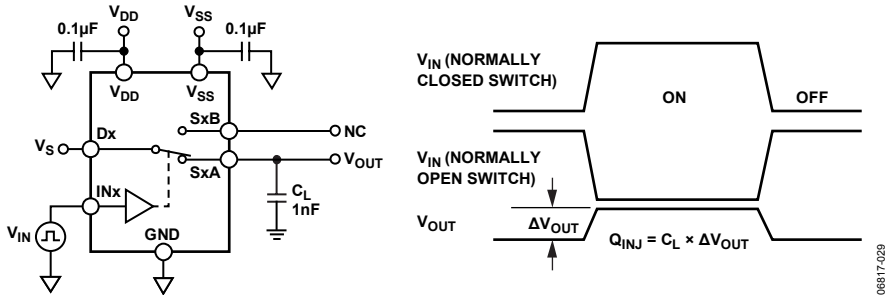

Figure 34. Charge Injection

OUTLINE DIMENSIONS

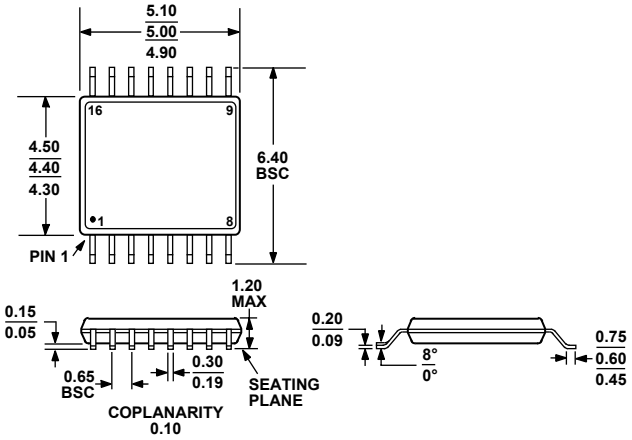

Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

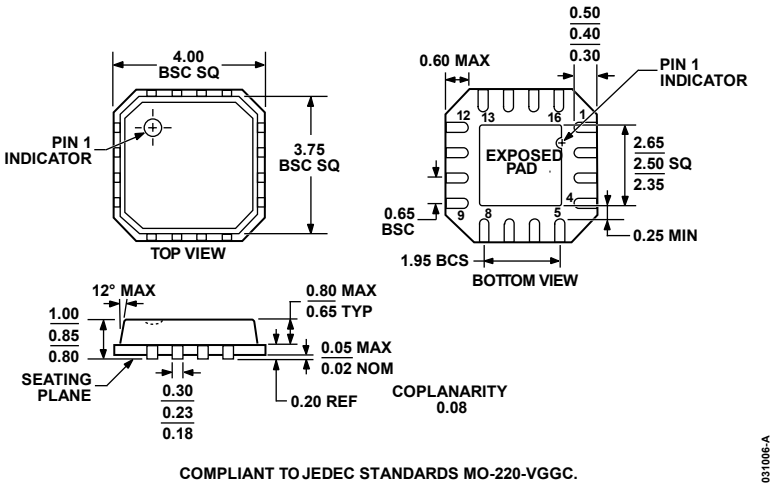

Figure 36. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1436YRUZ[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1436YRUZ-REEL7[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1436YCPZ-REEL[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-13
ADG1436YCPZ-REEL7[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-13

[1] Z = RoHS Compliant Part.

NOTES

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PR06817-0-8/07(PrD)